Abstract of the disclosure

A semiconductor integrated circuit comprises a plurality of data output pins, a test pin, a data processing circuit for generating output signals in response to input signals, and an output circuit for outputting the output signals to the data output pins in a normal mode and sequentially outputting each of the output signals to the test pin in response to a clock signal in a test mode. The test device includes only one test pin and the semiconductor integrated circuit may be tested by connecting the test pin of the test device to the test pin of the semiconductor integrated circuit. That is, the test device including only one test pin can test the semiconductor integrated circuit with n output pins.

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